PHASE I

FINAL TECHNICAL REPORT

Period of Performance: February 1, 1988 to July 31, 1988

TITLE:

Monolithic GaAS Digitzier for Space-base Laser Pulse Spreading Effect

Contract No: NAS5-30266

Sponsor:

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SUMMARY

An innovative 6-bit 1-GHz digitizer was designed to analyze the 1-ns pulse spreading effects in a space based altimeter. The digitizer consisted of four 4-bit flash A/D converters and a 6-bit encoder. Also, the converter utilized four 4-bit converters and a 4-to-6 bit encoder to achieve 6 bit resolution at the 1 GHz sample rate.

The design was unique because it utilized only the inverters and NOR gates for the converters and encoder, hence it could be fabricated using the existing state-of-the-art GaAs processing techniques.

This GHz digitizer has many commercial applications. It could be applicable to (1) digital microwave transmission system for the telecommunication industries, (2) pulse monitoring in high kinetic chemical reactions, (3) transient signals in the medical field and (4) microwave signals in astronomy.

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1.0 INTRODUCTION

This report describes studies of a low power, GHz 6-bit digitizer system utilizing state-of-the-art GaAs technology. The objective of this SBIR program was to design and simulate the performance of a monolithic GaAs 6-bit GHz digitizer for space altimeter applications. The anticipated hardware will be a digitizing system which accepts short (1-10 nanosecond duration) laser altimeter return pulses as the input, digitizes the signal at a GHz rate, demultiplexes the digital data down to MHz rates, and stores the data in RAM for access and analysis by simple 8-bit microcomputers.

The Phase I program was to perform a feasibility study of developing such a digitizer system for analyzing the spreading effect of 1-ns laser altimeter pulses. A system design was performed to define the functional blocks and circuits required, to perform the simulation of these circuit blocks, to define the system integration and the chip partitioning, to identify the GaAs foundry for the fabrication of the chips, and to estimate the performance and the power consumption of the digitizer.

The progress on the proposed tasks was discussed in the following sections. Section 4.1 covered system design and chip partitioning. A survey of GaAs foundries was performed and implementation of the proposed design using these fabrication facilities was discussed in Section 4.2. In Section 4.3, simulation results were presented. Performance estimates were given in Section 4.4.

2.0 TECHNICAL OBJECTIVES

The objective of this program was to perform a systematic study leading to the development of a monolithic GaAs 6-bit GHz digitizer for space altimeter applications. The specification for the digitizer system is shown in Table I.

Table I Target Sepcification for Digitizer

Maximum Input Signal	1 Volt
Input Impedance	50 Ohms
Sample Resolution	6-bit (16 mV)
Input Sample Rate	1 X 10^9 Samples/Sec.
Demultiplexed Output (4 Channels)	250 Megaword/Sec.
RAM Storage	128 Words (Min)
Output Interface	8-bit parallel
Physical Size	4" X 5" X 2" (Max)
Weight	0.5 Lb (Max)
Projected Cost (Quantity 1)	< $5000

In the Phase I program, the following tasks were performed:

Task 1: To perform a complete system design defining all the functional blocks and the circuits required.

Task 2: To perform the design and simulation of the comparator and the logic gates.

Task 3: To determine the optimal system integration of S/H and the A/D converter and chip partitioning.

Task 4: To identify the GaAs foundry that could fabricate the ICs in Phase II.

Task 5: To determine the performance and the cost for the digitizer.

3.0 TECHNICAL PROBLEM

Currently, NASA is constructing a prototype model of the Lunar Observer Laser Altimeter (LOLA) capable of continuously measuring the range to the lunar surface with submeter vertical resolution within a 30-300 m diameter surface footprint. This same instrument is also designed to provide a direct measure of the surface height distribution in the footprint by waveform analysis of the backscattered laser pulse. The wavelength of the altimeter is 1.06 microns. A short pulse (2 nsec) diode pumped Nd:YAG laser combined with a 25 cm diameter telescope, silicon avanlanche photodiode detector, ranging electronics, and instrument computer has been designed to make these measurements and meet all the requirements of the Lunar Geoscience Observer (LGO) mission. In the block diagram of LOLA system, as shown in Figure 1, a digitizer is needed which can achieve a nanosec resolution, 6 bit accuracy and can continuously process 100 nanosec time frames at a 50 Hz rate.

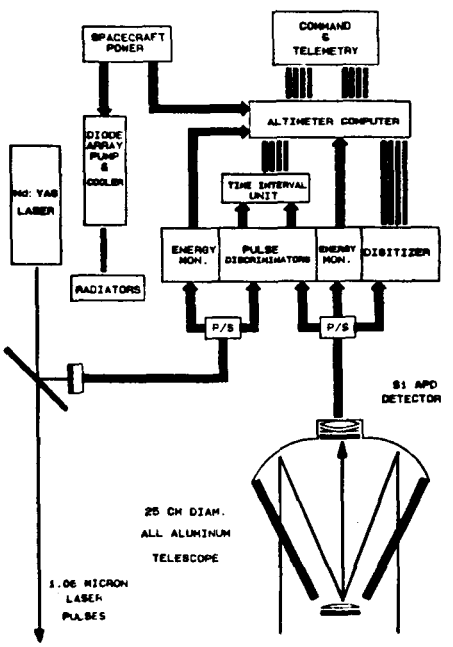

Figure 1- System diagram of the Lunar Observer Laser Altimeter.

4.0 STUDY RESULTS

4.1 System Design & Chip Partitioning

In Phase I an innovative design for a 1 GHz sample rate digitizer was performed based upon state-of-the-art high speed GaAs integrated circuits and interfacing to conventional micro-computers. The digitizer block diagram was shown in Fig. 2.

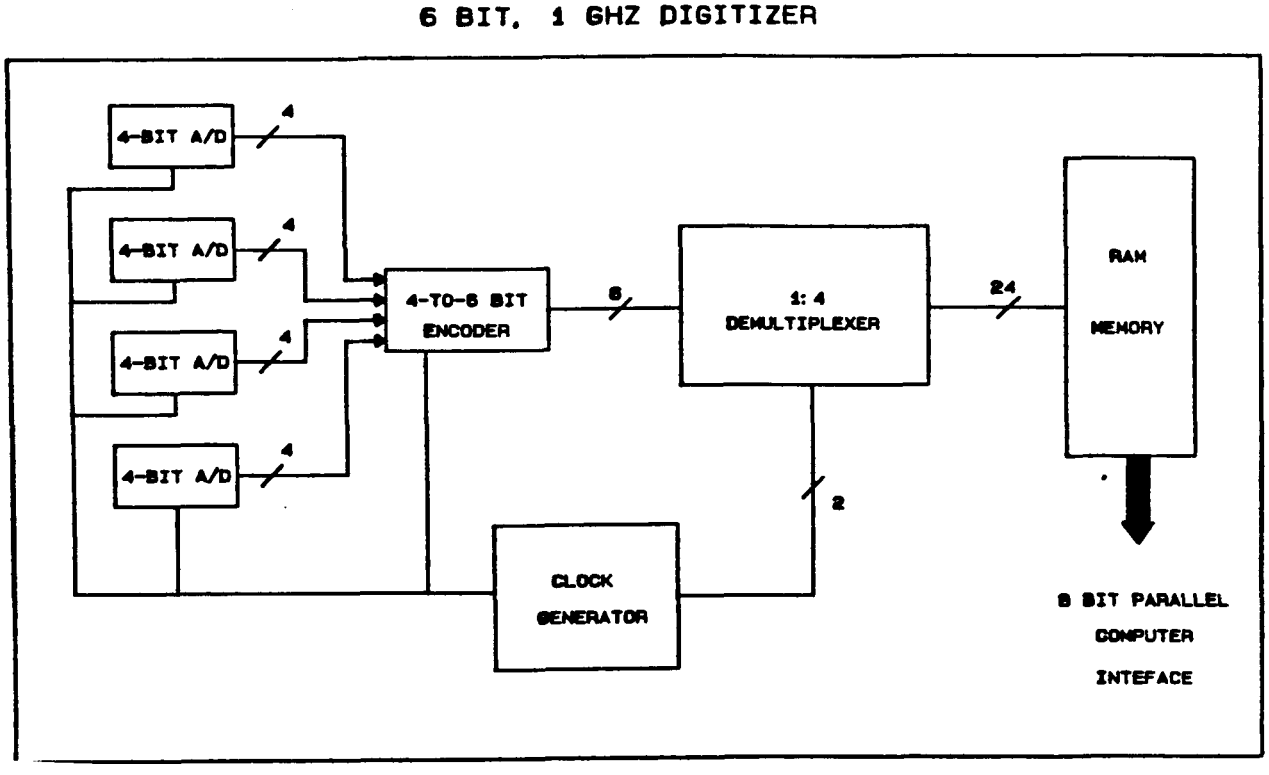

Figure 2- Block diagram of 6-bit GHz digitizer

This digitizer was separated into subsystem integrated circuits: 1) Four 4-bit GaAs A/D converters, 2) an encoder which took the four 4-bit A/D outputs and encoded them into a 6-bit word, 3) a 1-to-4 demultiplexer to reduce the data rate, 4) a random-access-memory for buffering the output to the altimeter computer, and 5) a high speed 1 GHz clock for synchronizing each of the subsystem elements. The A/D converter and decoder could

be fabricated using GaAs enhancement and depletion mode (E/D) technology.

4.1.1 4-bit A/D Converter

The 4-bit A/D converter, shown in Figure 3, consisted of 16 comparators, the output of which were encoded into a 4-bit word with an additional bit for carry. When four of these 4-bit A/Ds were used, the four 4-bit output words could further be encoded into one 6-bit word to form a 6-bit A/D converter. The repeated used of the simpler 4 bit decoder would minimize design time and layout errors.

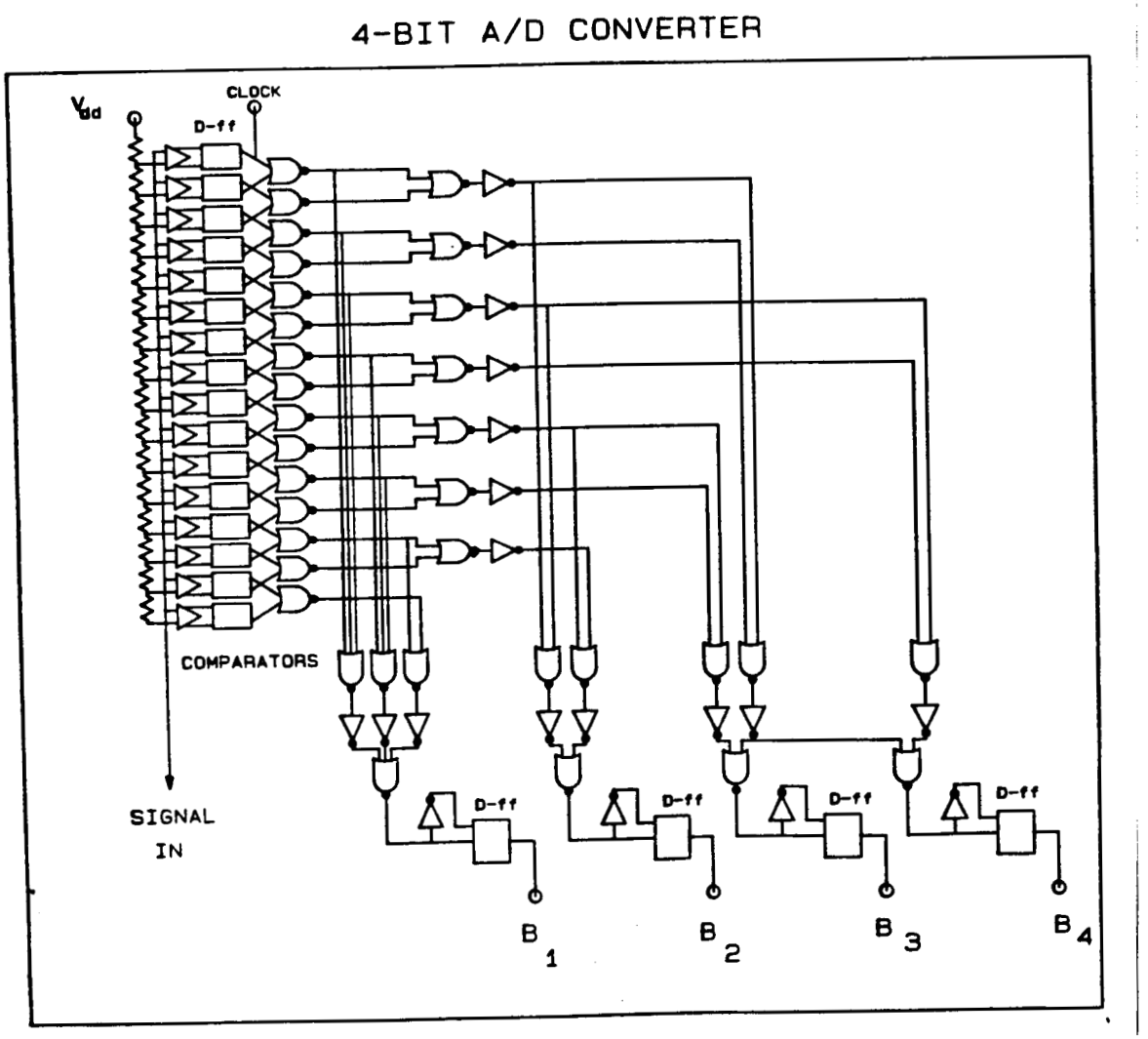

Figure 3- 4-bit A/D converter with 16 comparators

The design of the 4-bit A/D converters was such that the incoming signal was level-detected by the 16 comparators and encoded into a 4 bit word. Note here that only NOR gates, inverters and D flip-flops were used. This is a very important and innovative part of this design which makes the circuit realizable using current GaAs technology.

4.1.2 6-bit Encoder

The design of the 6-bit encoder, converting the four 4-bit words into a 6-bit output, was shown in Fig. 4. In addition

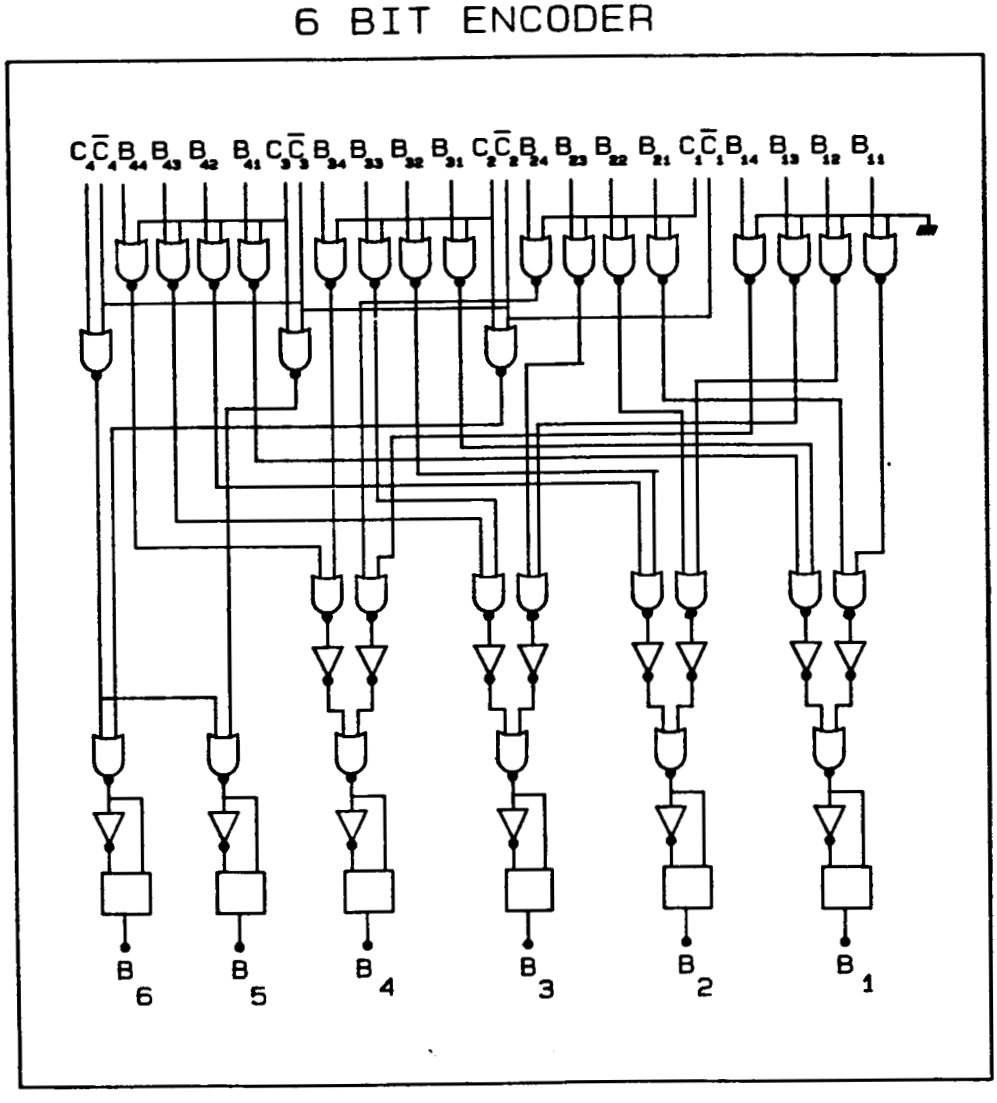

Figure 4- 6-bit encoder using the four 4-bit words

to using the four 4-bit words it also used the four top comparator outputs as the arithmetic "carry" in the encoding process.

The natural chip partitioning would be to separate the 4-bit D/A converter and the 4-to-6 bit encoder into two chips. The two chips would have about the same complexity, hence optimizing the yield. It also had the advantage of minimizing the design effort required because same circuit block (the 4-bit A/D converter) would be used repetitively in the system. Furthermore, in this system design, the 4-bit D/A converter chip could be a stand alone unit which would be used independently without the 4-to-6 bit encoder. In the final system integration, four 4-bit A/D chips would be used for each encoder chip. During masking, this ratio for the two chips could be maintained in the step-and-repeat process so that both chips in the 4:1 ratio were provided by a single mask set.

In this system design, the chip partitioning also made it possible to use 4-bit D/A converters available by other vendors. The risk and the amount of work for implementation in Phase II could further be reduced.

4.2 GaAs Foundry Selection

The GaAs foundries surveyed total 18. They were Adams Russell, Anadigics, Avantek, COMSAT, Ford, Gain Electronics, Harris Semiconductor, ITT, M/A Com, Microwave Semiconductor, Plessey, Sanders, Tachonics, Texas Instruments, TriQuint, and Varian, Vettesse, and Giga-Bit Logic. Because of the mix of analog and digital low power circuits required for the current program, enhancement and depletion (E/D) FETs are necessary in

order to achieve the low power consumption goal of around 1-watt.

E/D processes were available from Gain Electronics, ITT, TriQuint Semiconductor, Giga-Bit, and Vettesse. TriQuint was chosen as the primary foundry for the digitizer because it had the most complete process and device documentation and the stability of its process. Subsequently, the design manual, the device models, and the cell library were purchased from TriQuint in order to initiate circuit design and computer simulation.

4.3 Functional Block Definition & Simulation

The circuits in the 4-bit A/D converter and the encoder shown in Figs. 2 and 3 were designed with a minimum number of components. The main components needed were the comparators, inverters, NOR gates, and the D flip-flops. Typically, a given logic function such as an encoder could be implemented very simply if all five logic gates, inverter, OR, NOR, AND, and NAND were available. However, in the E/D logic family, only inverters and NOR gates could be designed effectively. While these two would be sufficient to implement all logic functions, the resultant circuitry was only slightly more complex than if all five gates were available. The innovation of the converter and the encoder design was that they were designed with only inverters and NOR gates for their digital sections. Thus they were realizable using today's state-of-the-art GaAs processing facilities.

The design method used for the GaAs circuits utilized the device equivalent circuit models for the TriQuint QED/A Process. The D-mode FET in this process had a threshold voltage of -Ø.6 while for an E-mode FET Ø.15. Besides, mixed mode device was

also available for power applications and switching with a threshold voltage of 2.0. Hence, all building blocks and circuit components were designed with D-mode and E-mode devices.

The NOR gate design is shown in Fig. 5. It consisted of two parallel inputs A and B in an inverter configuration. The load of the inverter was active and used a D-mode FET. The output of the inverter was buffered by a source follower for low impedance fan-out capabilities. The diode level shifter in the input was to allow the input signal to effectively turn off the input E-mode FETs. The inverter design was similar to the NOR gate design with only one input FET. Both the inverter and the NOR gate had been computer simulated with the SPICE program.

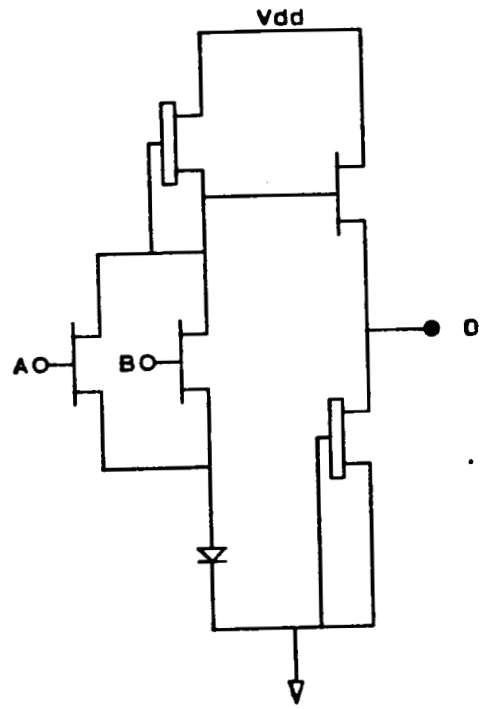

Figure 5- NOR gate design with E/D process

In Fig. 6, the solid line showed the input and output voltage relationship of the inverter. The dashed line was with

the input and output relationship reversed.

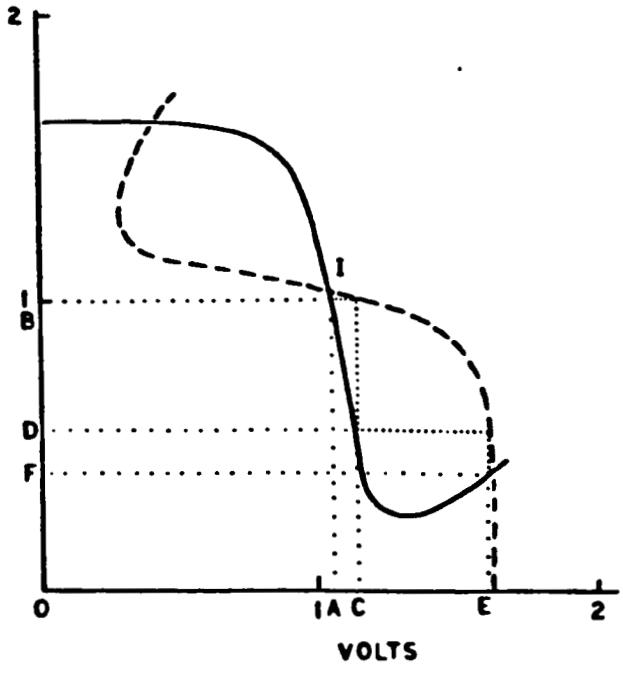

Figure 6- Inverter response and noise margin

The two large loops formed by the two curves indicated very good noise margin for the inverter design. Let, for example, a number of inverters be connected in series as shown in Fig. 7 with A, B, and C as the output nodes. If a logic high input, very

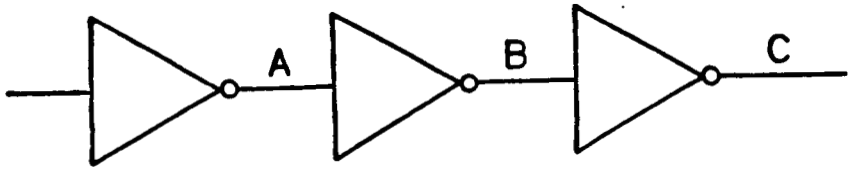

Figure 7- Inverters in series

close to the intersecting point I, was applied to A, then the outputs B and C would progressively move away from I making the

logic level more distinct and less ambiguous as shown by the stair case curve. For critical path analysis, the gate delay through an inverter or equivalently a NOR gate was important. The computer simulated transient response of an inverter for a pulsed input was shown in Fig. 8. The fall time delay is around 40-ps while the rise time delay 120-ps.

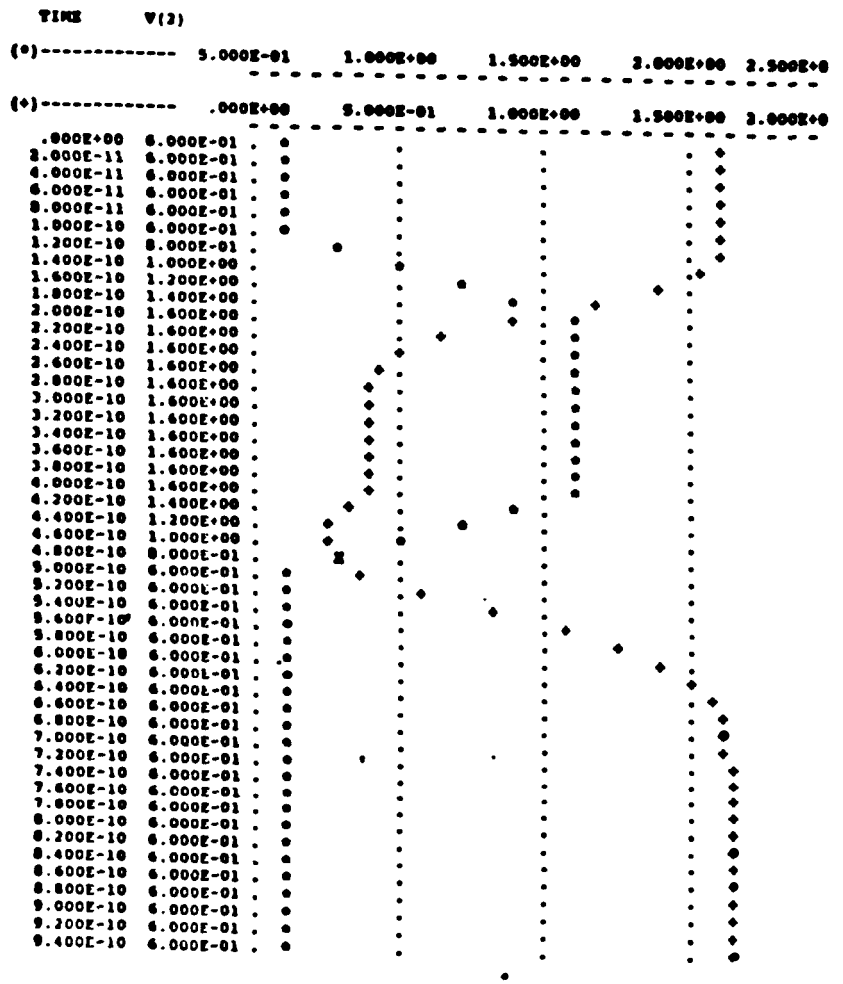

Figure 8- Rise and fall time gate delay of an inverter

The D flip-flop required in the circuit was designed with the six NOR gate configuration as shown in Fig. 9.

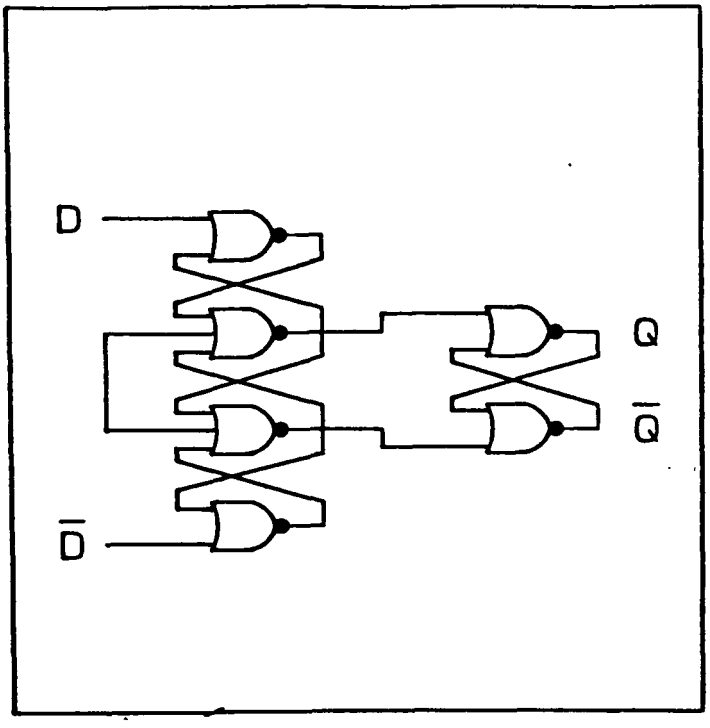

Figure 9- Six NOR gate D flip-flop

The simulation of the D flip-flop was performed with the standard divide-by-two circuit configuration where the D-input is connected to the Q output and similarly for the inverted input and output. The output frequency was then half of the clock frequency, as shown in Fig. 10. The propagation delay was about 480-ps.

The key analog component of the D/A converter was the comparator. It had to convert a small voltage differential into a full logic signal, which implies large voltage gain. Several versions of the comparator had been studied and simulated. Most did not have the required gain to function effectively. The final version had a master-slave structure which used a positive feedback in the slave section to achieve the desired gain. The schematic of the comparator was shown in Fig. 11.

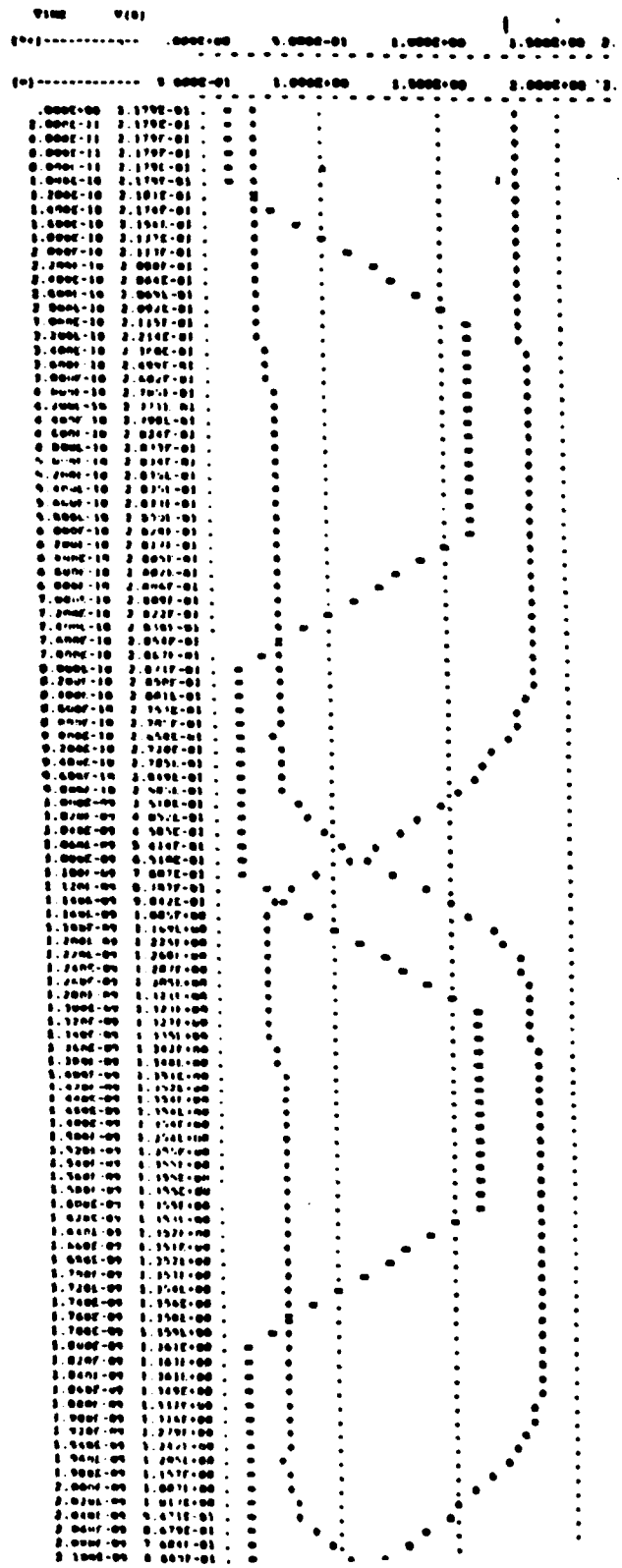

Figure 1Ø- Simulated output of the D flip-flop as a div-by-2

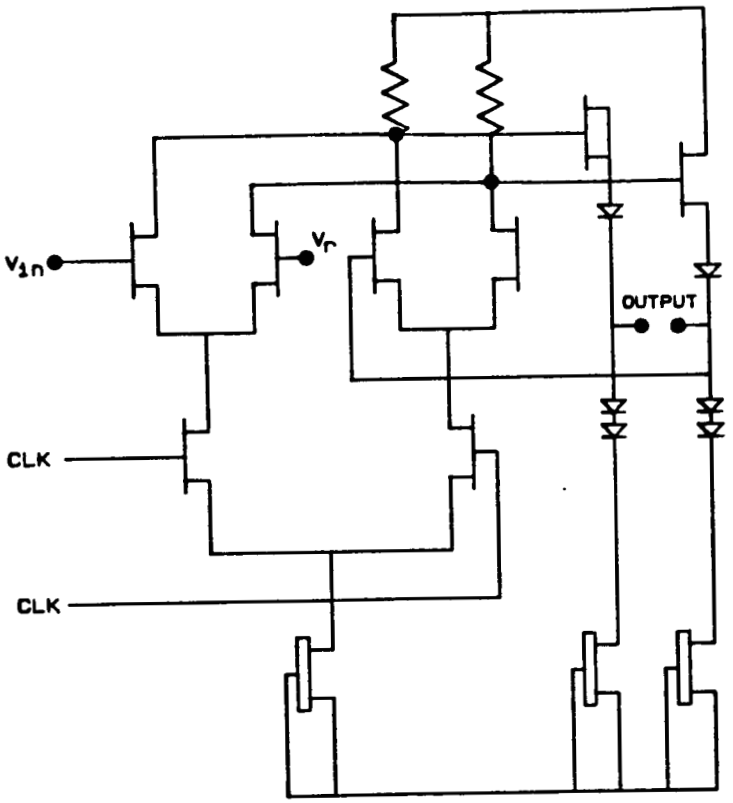

Figure 11 Schematic of the comparator

Computer simulation of its performance was shown in Fig. 12. For the differential inputs of the comparator, one input was a constant voltage of 2.5-V while the other input, denoted by (*) in Fig. 11, was a triangular waveform with an amplitude of 10-mV around the reference voltage of 2.5-V. The clock pulse signal at 1-GHz was indicated by (+) while the output of the comparator, valid only when the clock was low, was denoted by (=). At the falling edge of the clock signal (+), data was transferred from the master comparator to the slave latch. Clearly, less than 10-mV input differential voltage was sufficient to trigger the comparator output. The input signal swing was expected to be around 1-V. The required 6-bit voltage resolution was 16-mV. Hence the comparator gain resolution was sufficient for the 6-bit A/D converter application. In fact, the limiting factor for the comparator voltage resolution was the material-related threshold

voltage hysteresis and inhomogeneity rather than the minimum triggering voltage of the circuit.

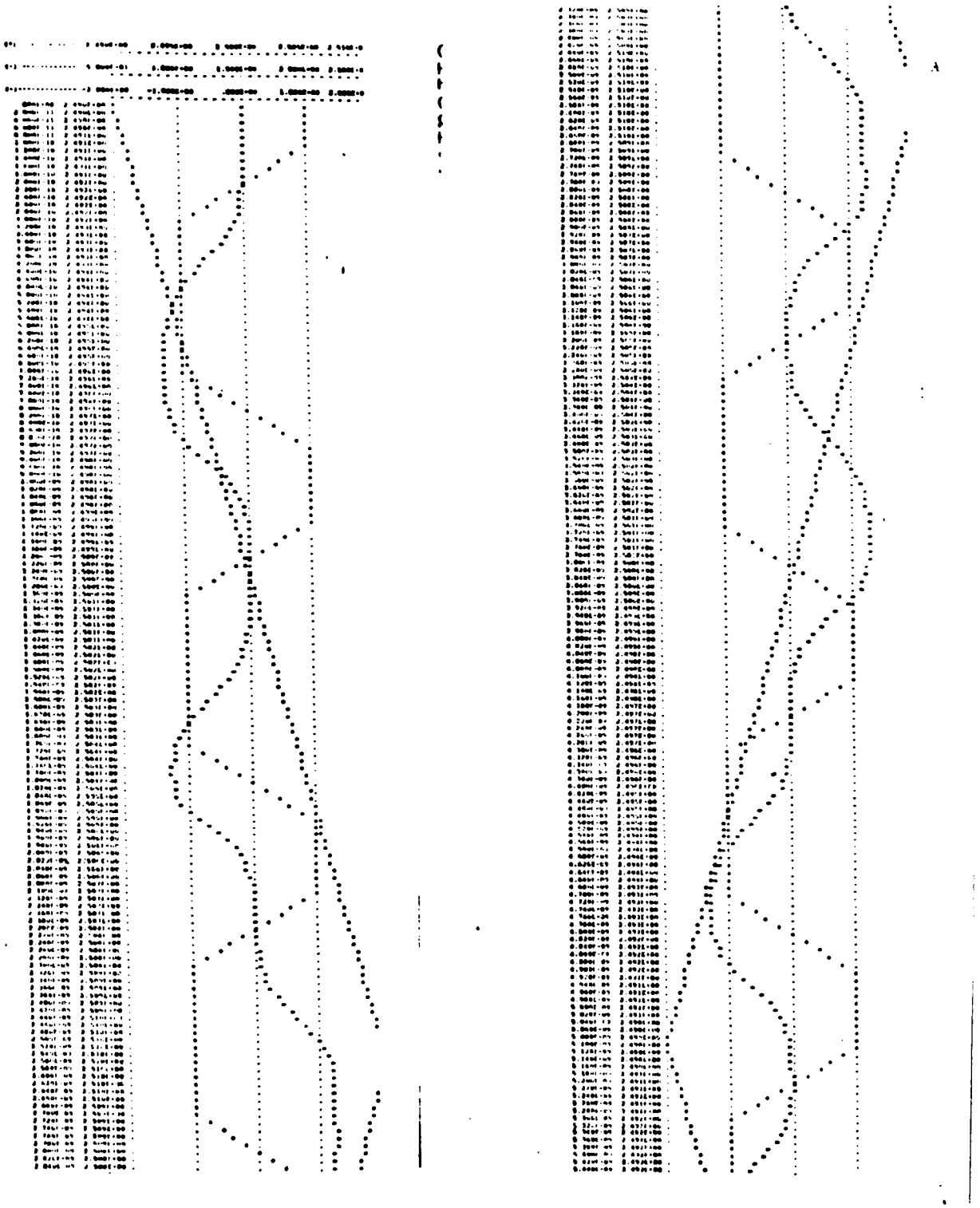

Figure 12- Simulation of comparator performance

4.3.1 RAM Buffer Memory

A 4:1 demultiplexer and a random access memory (RAM) buffer memory was designed to provide temporary storage for the high speed data and allow a relatively slow external 8-bit computer to access the acquisition data. The subsystem architecture was shown in Figure 13. The 1 GHz sample clock was divided by 4 to generate

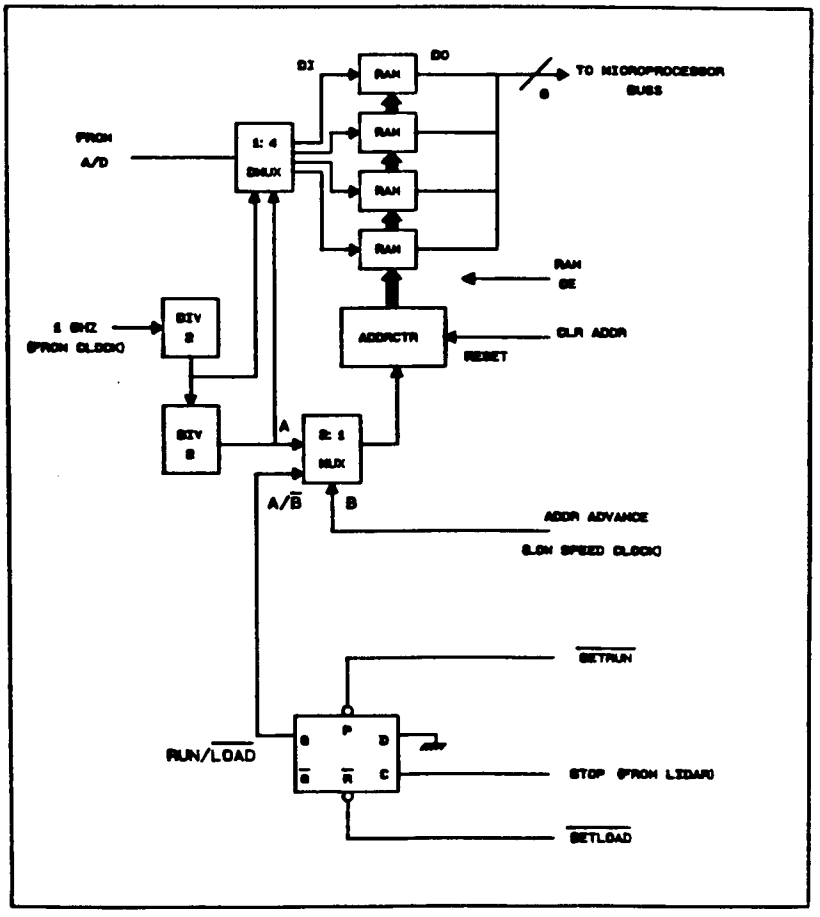

Figure 13- RAM Buffer Memory and demultiplexer providing interfacing to a relatively slow 8-bit computer.

demultiplexer control signals and to distribute the data samples into 4 parallel streams at 250 MHz. The 250 MHz clock was used to increment a high speed counter which in turn generated addresses for the GaAs RAMs. The GaAs RAM and demultiplexer circuits were available commercially (Vittesse and Giga-Bit

Logic) and thus would be used in the Phase II implementation.

When the supervisory processor (of the altimeter computer) asserted the SETRUN signal, the 2:1 multiplexer fed the high data rate signal to the counter. Upon a STOP signal from the altimeter computer, the MUX switched the counter to use address advance signals from the supervisor processor. The supervisor processor could assert the RAM output enabling to read the RAM contents. By alternately asserting ADDR ADVANCE and RAM OE, all of the stored bytes were read out to the altimeter computer. The various supervisory signals were derived from buss control signals using programmable array logic (not shown) to decode addresses and strobes appropriately.

4.4 Performance Estimate

All the computer simulations had been performed with a clock frequency of 1-GHz. The gate delays had also been found to be less than 500-ps. An A/D converters could, therefore, be designed with these building blocks to perform to 1-GHz rate. The comparator had been designed as a synchronous circuit. It was clock-driven by the main GHz clock and simultaneously sampled and latched the input waveform only at the falling edge of the clock signal. The power consumption break-down was estimated to be as follows: The comparators at 2.4-mW each consumed 153-mW. 259 inverters and NOR gates at 2-mW level were 518 mW. The D flip-flops at 12-mW per gate would use 216-mW. The total power would be about 887-mW. There were a number of interstage buffers, input and output buffers and clock buffers with an overhead power budget of 25% of the total.

The cost of the circuits were difficult to estimate because of the uncertainty in the die yield. In low production quantities with $2000 per wafer and 30% yield, the unit die cost would be $7 per circuit. The testing and packaging cost could increase the cost to about $200 per circuit. A total estimated digitizer cost in low volume quantities is estimated to be $5000.

5.0 CONCLUSION AND RECOOMENDATION

In Phase I, a miniature, low power, GaAs monolithic GHz waveform digitizer was designed for analyzing space-base laser altimeter pulse spreading effect. It consisted of a 6-bit GaAs flash A/D converter using the enhancement/depletion (E/D) technology with latching comparators, a demultiplexer to reduce output data rate and a surface acoustic wave (SAW) oscillator for the GHz clock.

The results of the feasibility study confirmed that: 1) The E/D GaAs technology minimized the power consumptions of the 6-bit A/D converter to less than 1 watt, 2) the E/D latching comparators provided high gain and reduced the comparator off-set voltage down to 15 mV, thus making the 6-bit dynamic range realizable, 3) the demultiplexer made the GaAs data stream accessible to low speed memories and processors, and 4) the GHz SAW oscillator provided a stable clock signal with low power drain because of the elimination of a frequency multiplier chain.

Based on the studies of Phase I, it is recommended that a hardware demonstration model be developed. It is further recommended that the development of a prototype digitizer system be integrated into the Lunar Observer Laser Altimeter (LOLA) system.